AGMPA086135

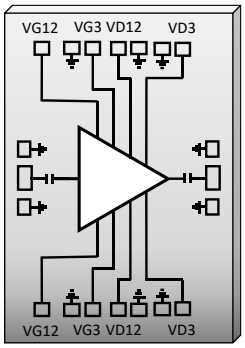
GaAs MMIC
1.5W 9.5-13.3GHz Power Amplifier

Typical Applications

- Point to Point Radio
- X-Band Communications
- Radar

Features

- Frequency Range: 9.5 – 13.3 GHz
- Gain: 32dB
- PSAT: 32.5dBm
- PAE: >30%
- IM3: - 40dBc @ 19dBm/Tn
- Bias: +6V @ 840mA
- 50Ω Matched Input / Output
- RF Input / Output DC blocked
- Die Size 3.0 x 2.0 x 0.1 mm





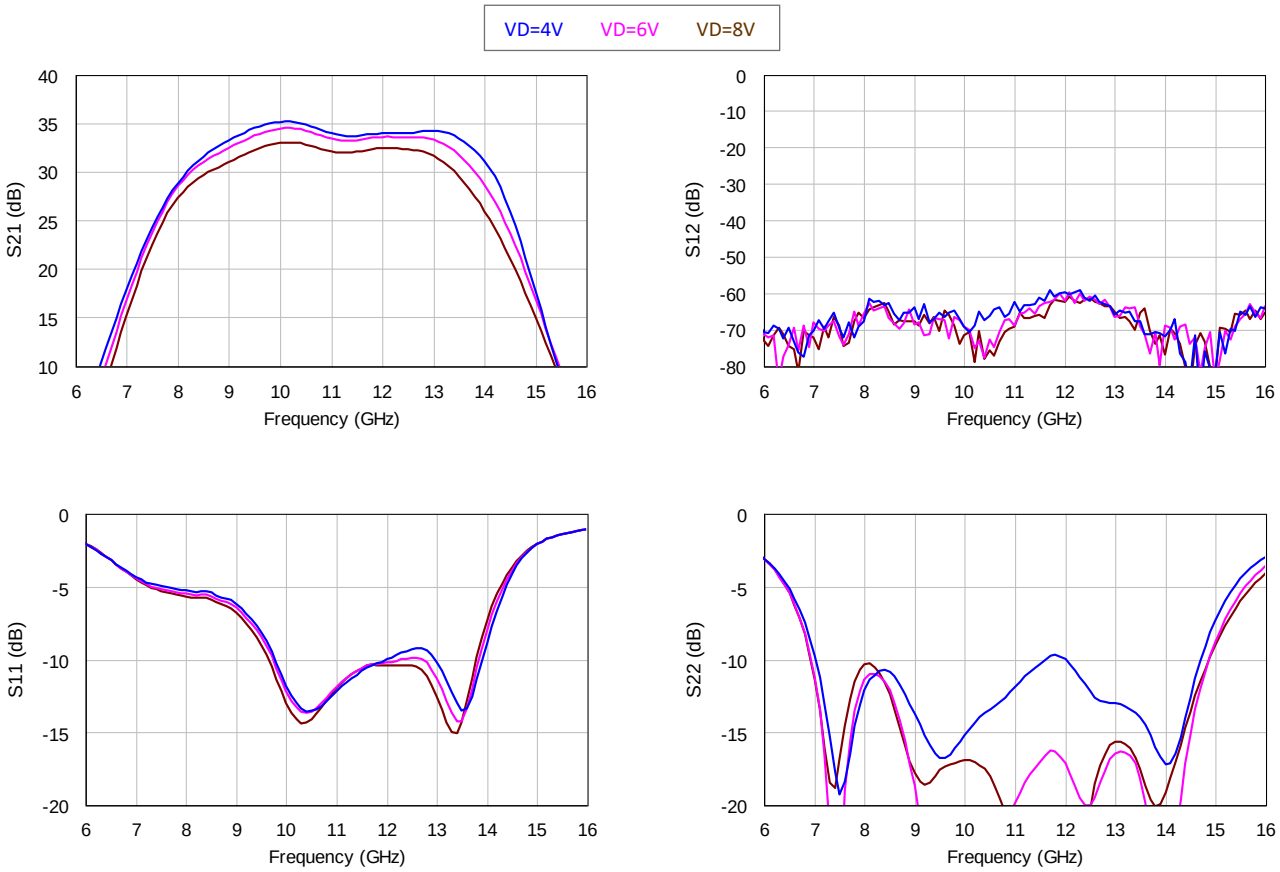
Electrical Specifications (TA = +25°C, VD = +6V, IDD = 840mA)

Parameter	Units	Minimum	Typical	Maximum
Frequency	GHz	9.5		13.3
Gain	dB		32	
Gain Flatness	dB		± 0.5	
Input Return Loss	dB		10	
Output Return Loss	dB		10	
Psat	dBm		32.5	
PAE	%		30	
IM3 @ 19dBm/Tn	dBc		-40	
Supply Voltage	V		+6	
Supply Current	mA		840	
DC Dissipated Power	W		5.04	
Package Type			Die	

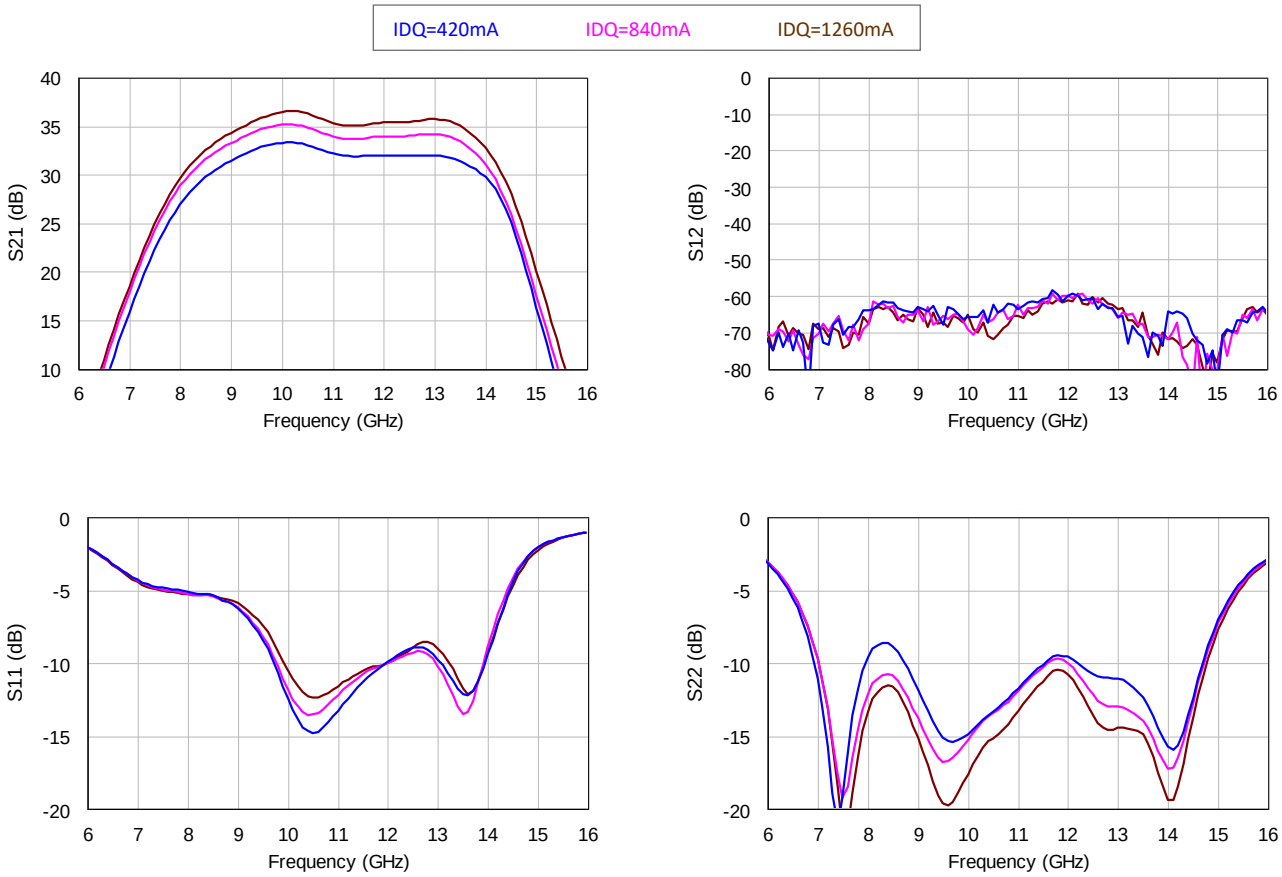
Power Amplifiers

Performance Graphs

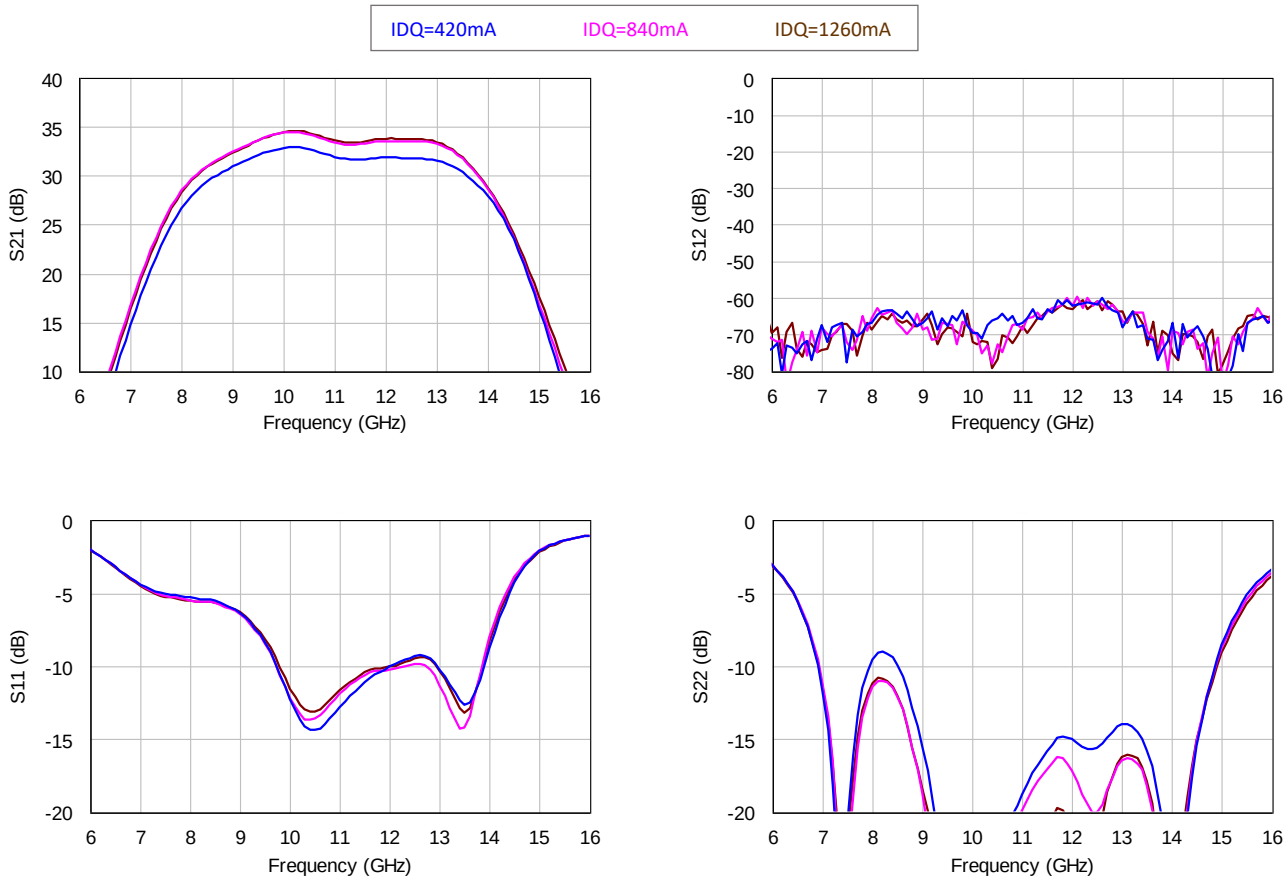
S-Parameters vs. VD (25°C, IDQ=840mA)



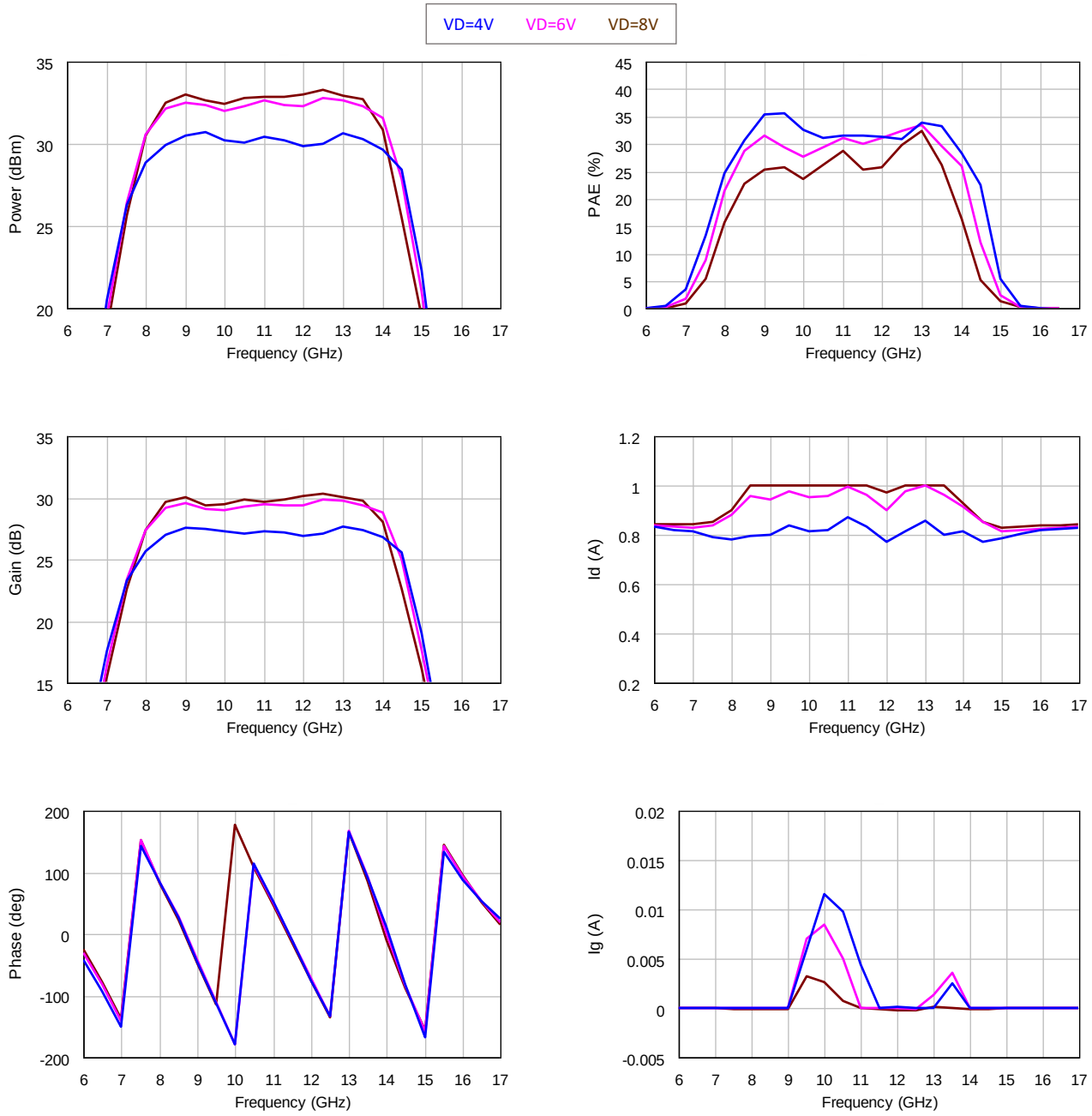
S-Parameters vs. IDQ (25°C, VD=4V)



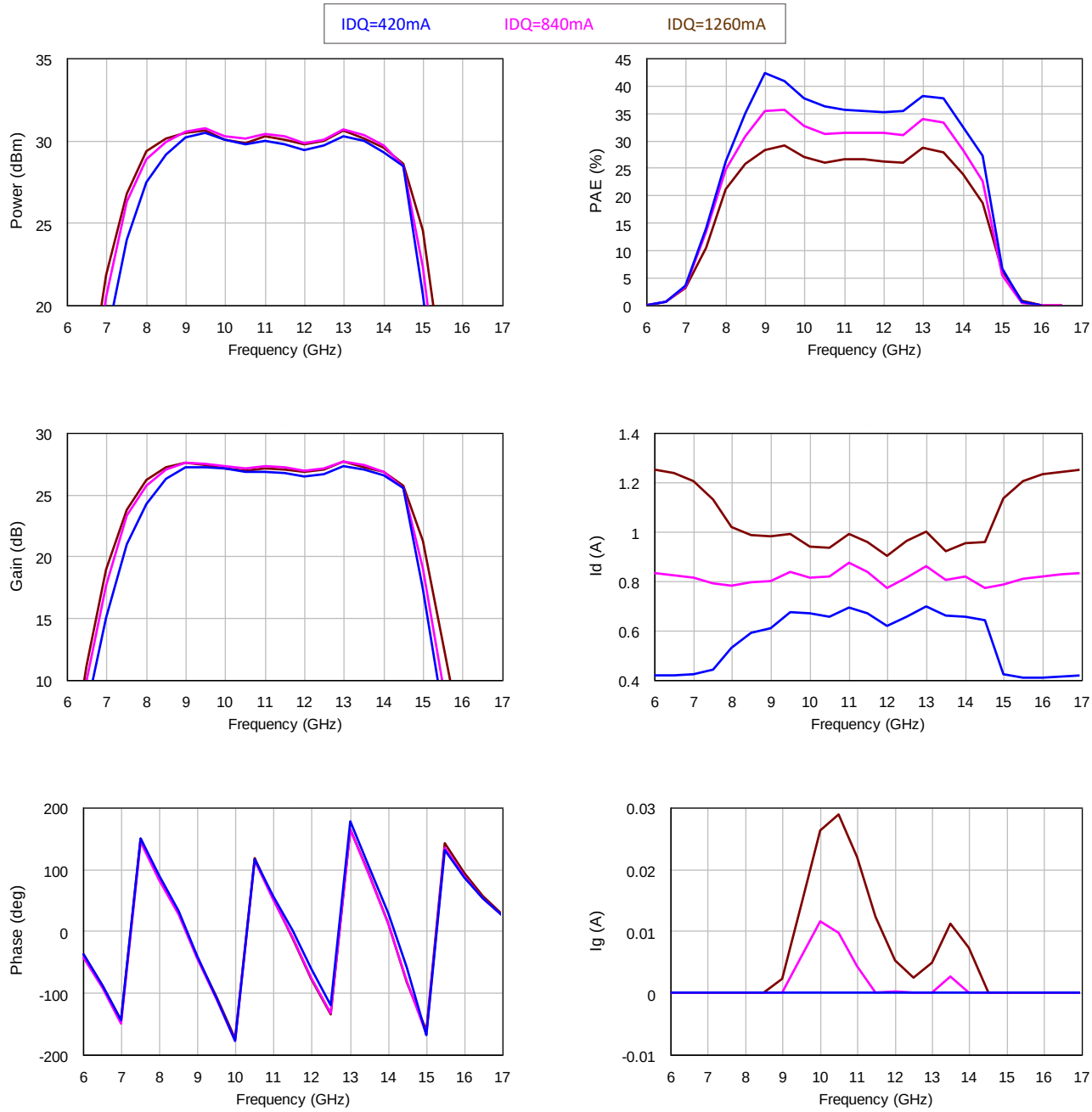
S-Parameters vs. IDQ (25°C, VD=6V)



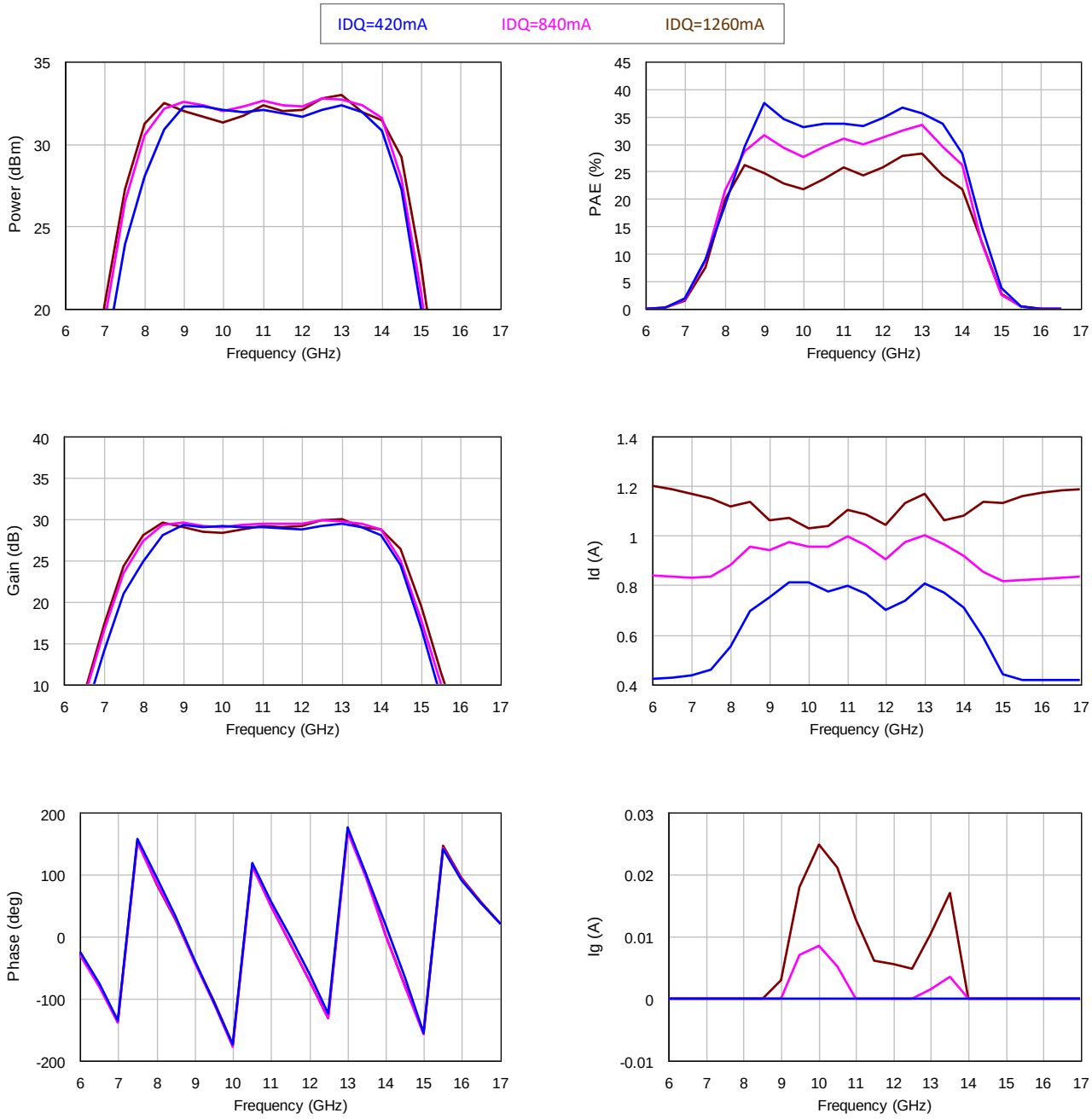
Frequency Response vs. VD (25°C, IDQ=840mA, Pin=+3dBm)



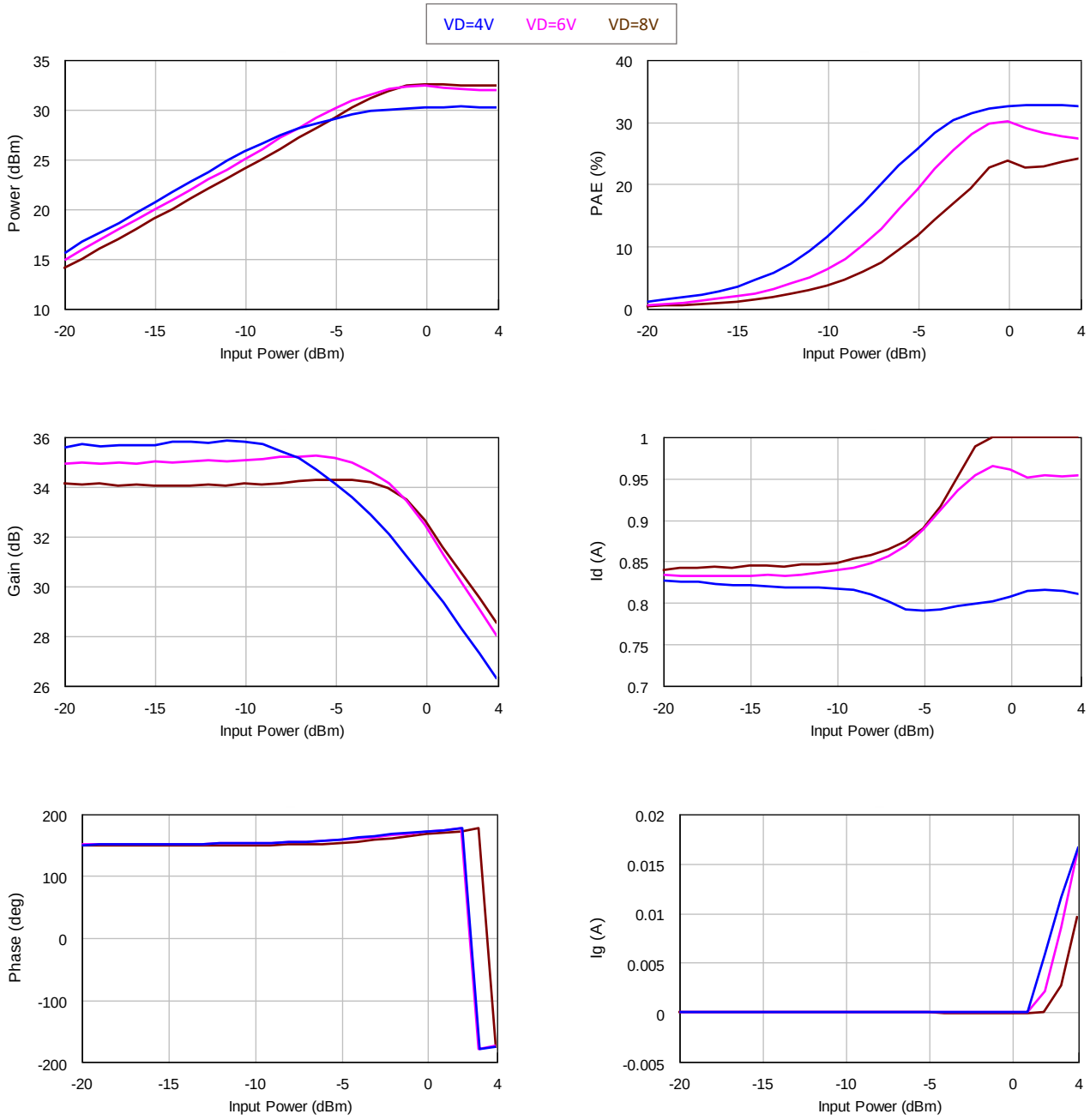
Frequency Response vs. IDQ (25°C, VD=4V, Pin=+3dBm)



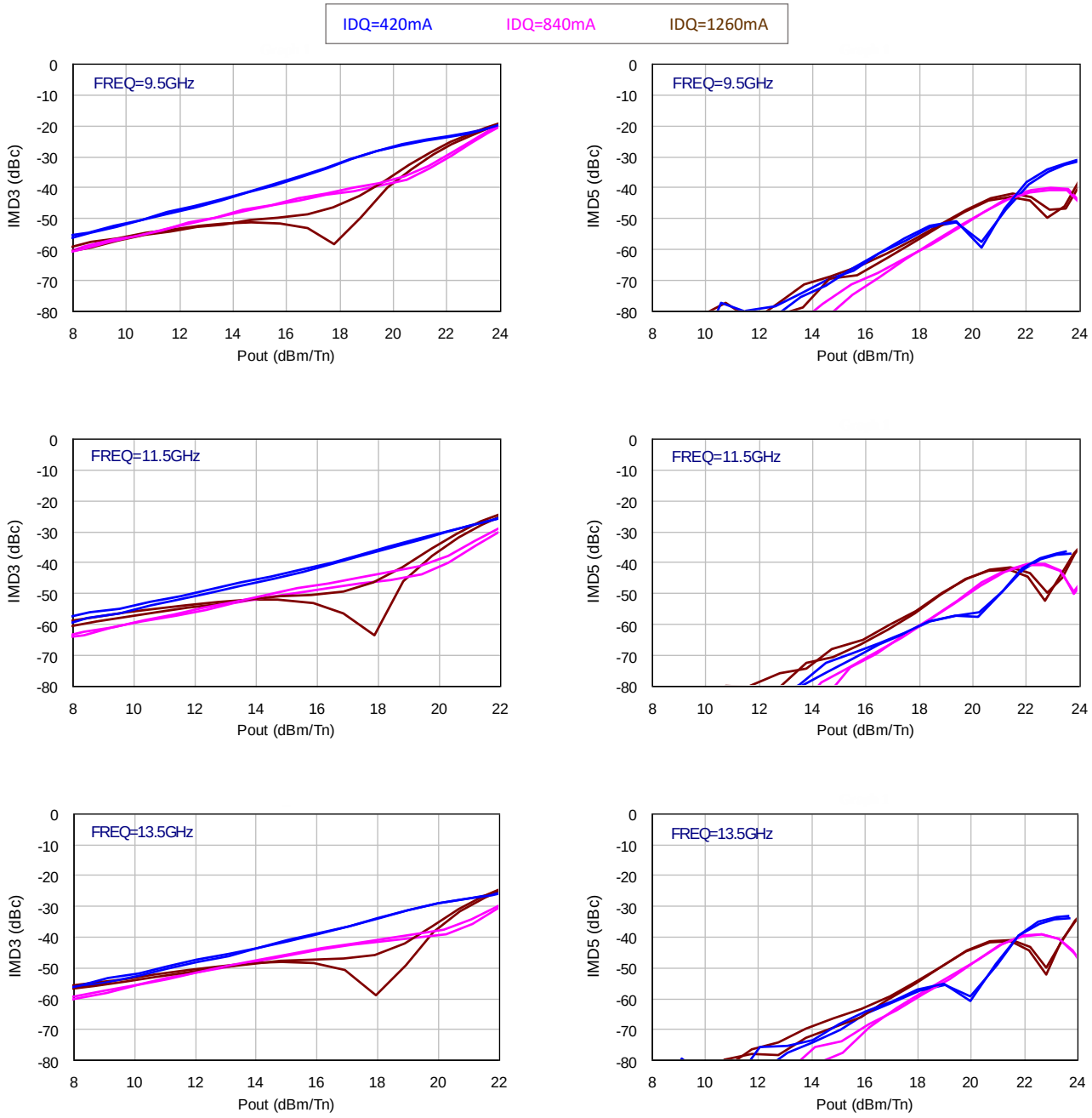
Frequency Response vs. IDQ (25°C, VD=6V, Pin=+3dBm)



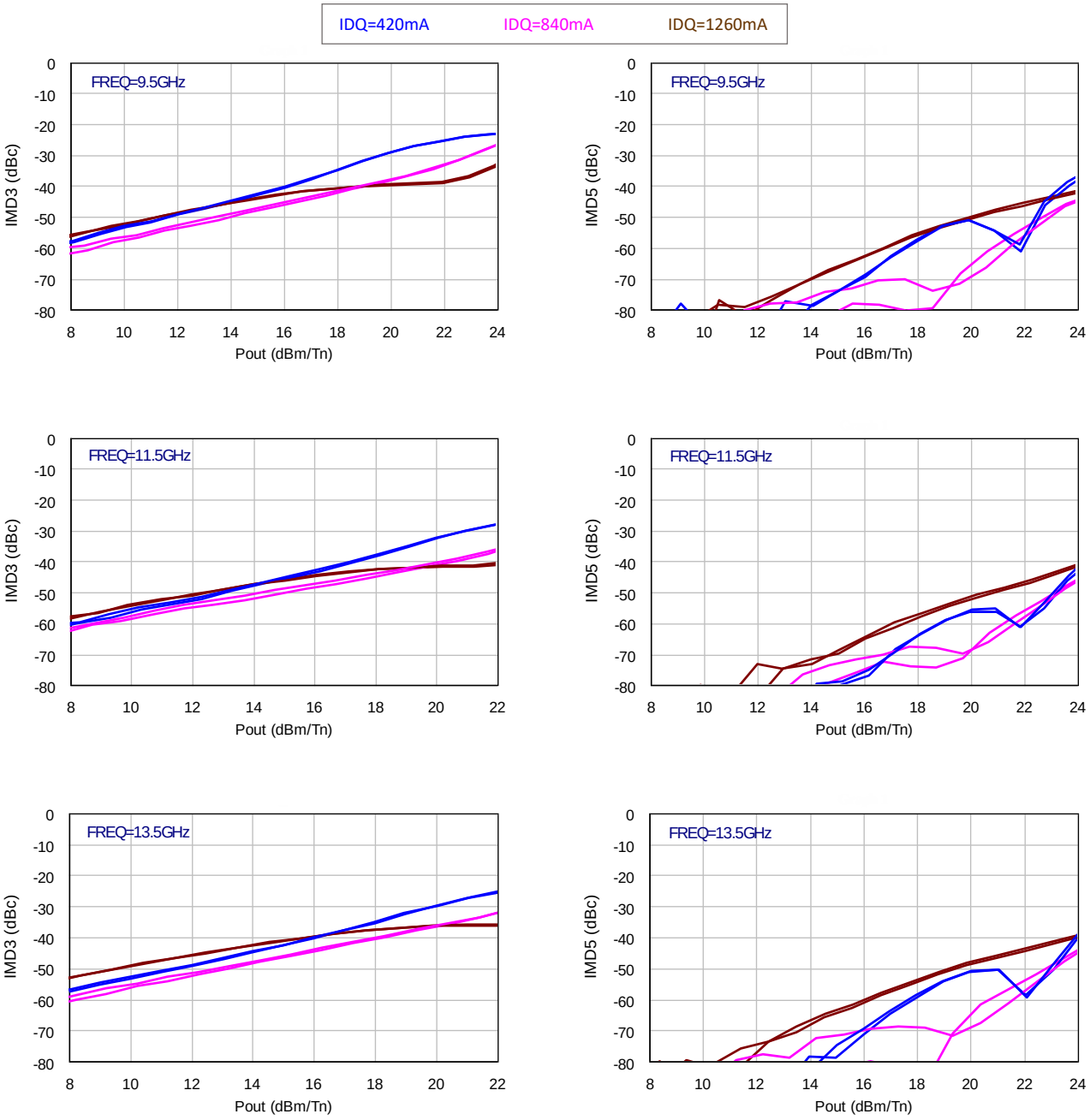
Power Sweep vs. VD (25°C, IDQ=840mA, Freq=11.5GHz)



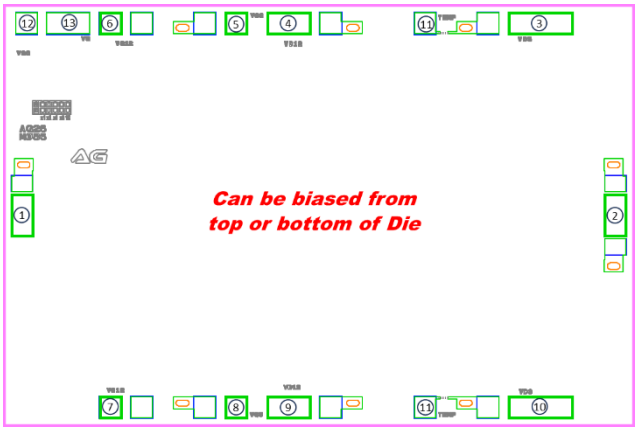
Linearity Response vs. IDQ (25°C, VD=4V, 10MHz Tone Spacing)



Linearity Response vs. IDQ (25°C, VD=6V, 10MHz Tone Spacing)



Die Outline Drawing

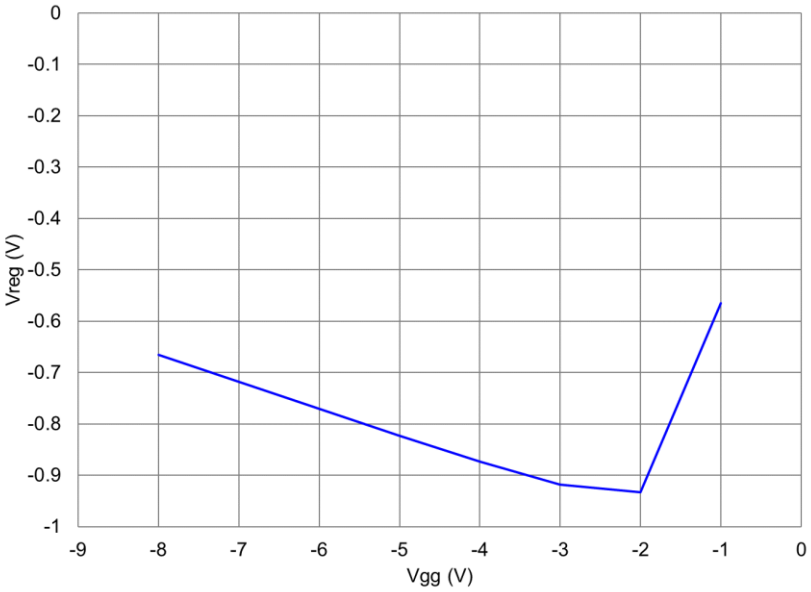


Die Pad Descriptions

Pad	Function	Pad Size	Description
1	RFIN	100x200µm	AC coupled 50Ω Matched
2	RFOUT	100x200µm	AC coupled 50Ω Matched
3	VD3	300x100µm	Drain Power Supply voltage, bypass capacitors needed*
4	VD12	200x100µm	Drain Power Supply voltage, bypass capacitors needed*
5	VG3	100x100µm	Gate Power Supply voltage, bypass capacitors needed*
6	VG12	100x100µm	Gate Power Supply voltage, bypass capacitors needed*
7	VG12	100x100µm	Alternate Gate Power Supply voltage, bypass capacitors needed*
8	VG3	100x100µm	Alternate Gate Power Supply voltage, bypass capacitors needed*
9	VD12	200x100µm	Alternate Drain Power Supply voltage, bypass capacitors needed*
10	VD3	300x100µm	Alternate Drain Power Supply voltage, bypass capacitors needed*
11	TProbe	100x100µm	Monitor Temperature
12	VGG	100x100µm	Alternate Gate Power Supply voltage (See Plot)
13	Vreg	200x100µm	Alternate, Gate Voltage Regulator Output (See Plot)
Die Bottom	GND	Backside	Epoxy/Solder to Baseplate

*See Assembly Diagram

On-Chip Gate Regulator Performance (Optional Connection)

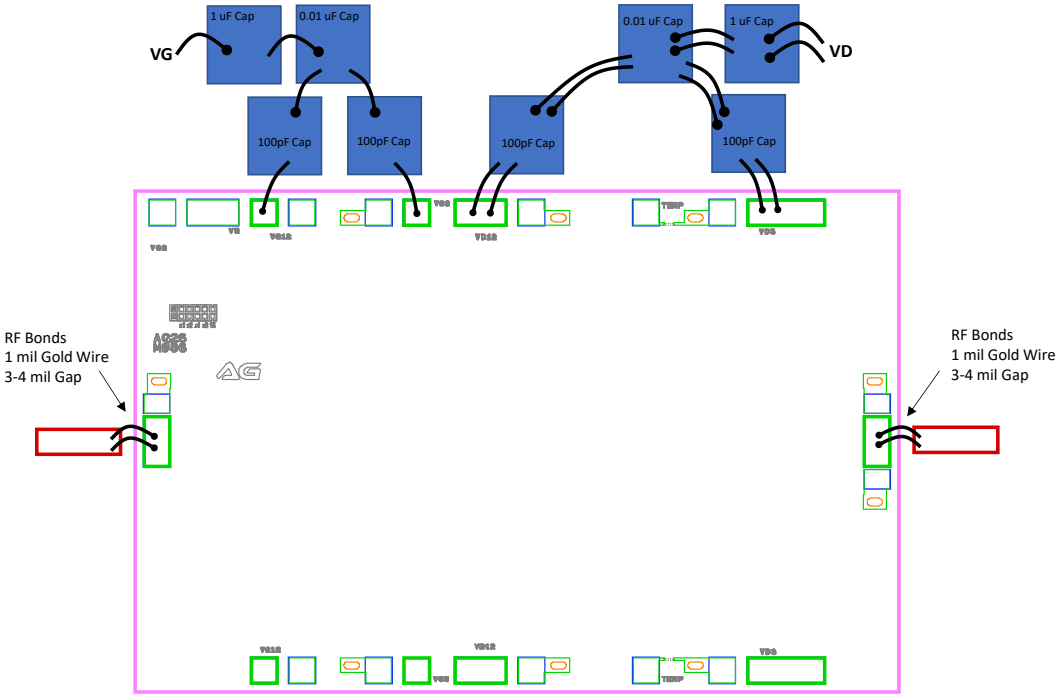


Absolute Maximum Ratings

Parameter	Rating
Drain Bias Voltage (VDD)	+8V DC
RF Input Power (RFIN)	+20dBm*
Channel Temperature	150°C
Storage Temperature	-65 to 150°C
Operating Temperature	-55 to 85°C

*To be tested

Die Assembly Diagrams



Die Assembly Notes:

1. Die Thickness is 100µm
2. Backside and Bondpad metallization: 4µm gold
3. High K Silver Epoxy or AuSn Eutectic attach MMIC
4. Gap between MMIC and 50 Ohm lines should be 3-4mils
5. Off-Chip bypass capacitor values are approximate



Die Packaging Information

- GP-4 (Gel-Pak)

Biasing and Operation

The AGMPA086135 is biased with a positive drain supply and negative gate supply. Performance is optimized when the drain voltage is set to Vdq. The preferred biasing procedure is as follows:

Turn ON procedure:

1. Set VG to -1.0V.
2. Set VD to Vdq.
3. Adjust VG more positive until Id = Idq.
4. Apply RF signal.

Turn OFF procedure:

1. Turn off RF signal.
2. Reduce VG to -1.0V. Id should be 0mA.
3. Turn off VD.
4. Turn off VG.

Important Notice

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