AGLNA013048

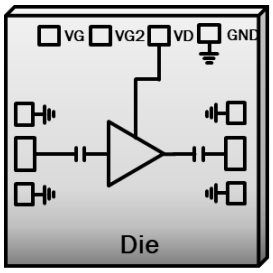
InGaAs pHEMT MMIC
2.0 – 4.0GHz Low Noise Amplifier

Typical Applications

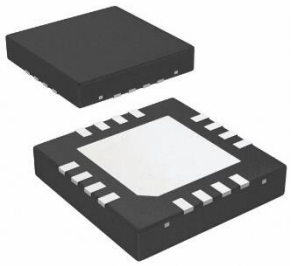
- Test Instrumentation
- S-band Radios
- Telecom Infrastructure
- 5G Base Stations

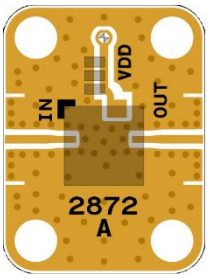
- Frequency Range: 2.0 – 4.0 GHz
- Noise Figure: 0.7dB
- Gain: 32.5dB
- P1dB: + 11.6dBm
- Self-Biased: +4V @ 31mA Single Supply
- 50Ω Matched Input / Output DC blocked
- X-MWblocks available

Features









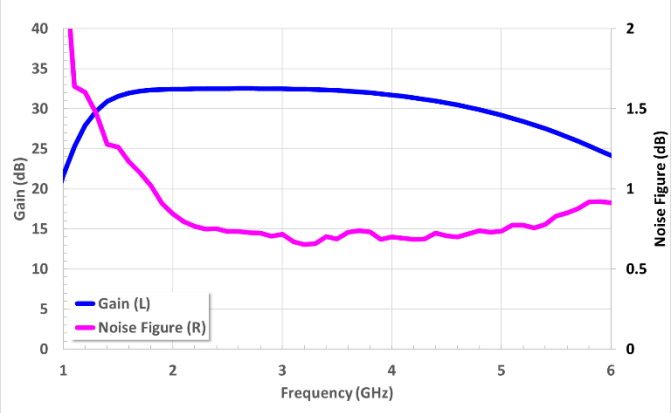
Part#	Packaging
AGLNA013048	Die 1.8 x 1.8 x 0.1 mm
AGLNA013048Q	QFN 4x4 16Lead
XM-D6C5-0304D	X-MWBlock with QFN

Electrical Specifications (TA = +25°C, VD = +4V, IDD = 31mA)

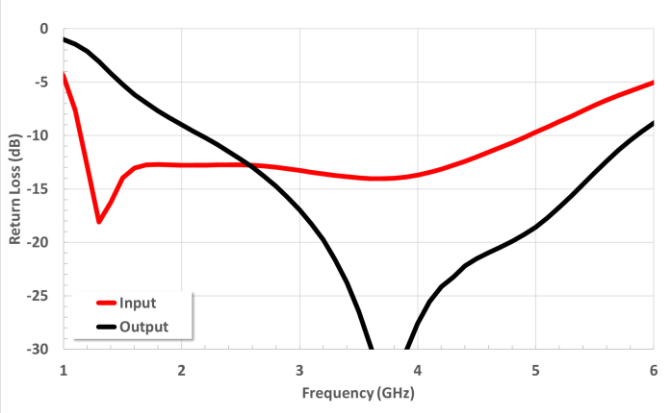
Parameter	Units	Minimum	Typical	Maximum
Frequency	**GHz**	**1.3**		**4.8**
Gain	**dB**		**32.5**	
Gain Flatness	**dB**		**± 0.5**	
Noise Figure	**dB**		**0.7**	
Input Return Loss	**dB**		**13**	
Output Return Loss	**dB**		**10**	
P1dB	**dBm**		**13**	
Psat	**dBm**		**13.5**	
Supply Voltage	**V**		**+4**	
Supply Current	**mA**		**31**	
DC Dissipated Power	**mW**		**150**	
Package Type			**Die/QFN**	

Die Performance Graphs

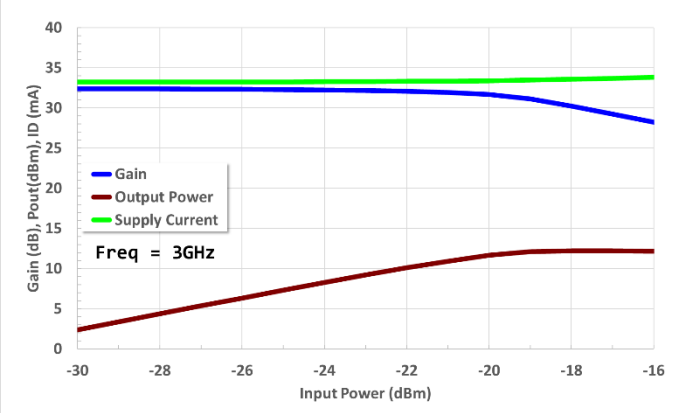
Gain and Noise Figure



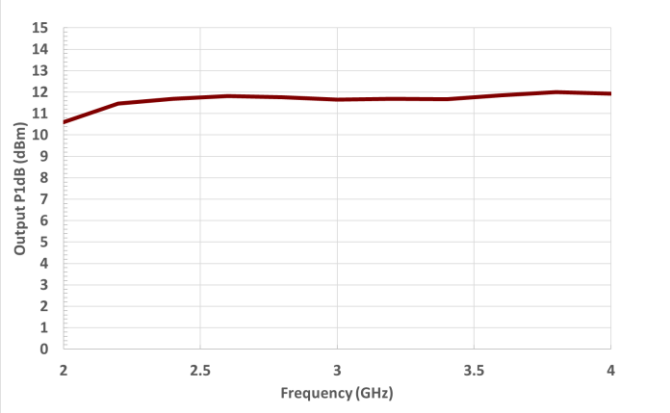
Return Losses



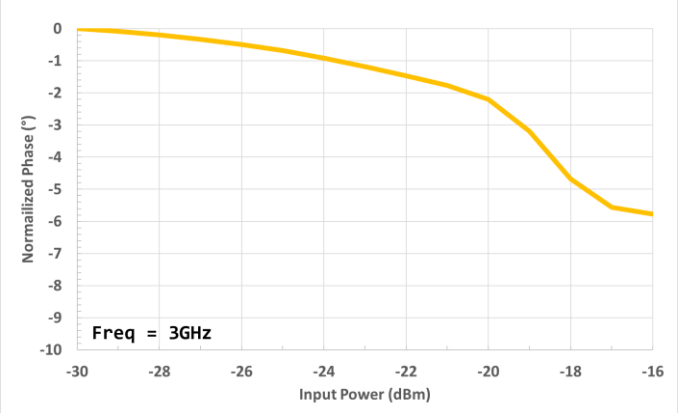
Power Sweep



Power Out P1dB



AM to PM

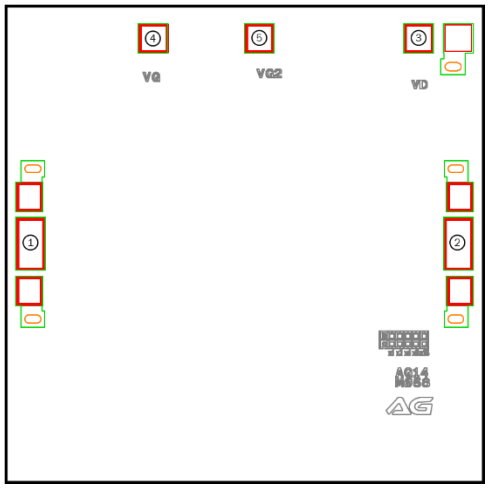


Low Noise Amplifiers

AGLNA013048

InGaAs pHEMT MMIC
2.0 – 4.0GHz Low Noise Amplifier

Die Outline Drawing



Die Pad Descriptions

Pad	Function	Pad Size	Description
1	RFIN	111x200µm	AC coupled 50Ω Matched
2	RFOUT	111x200µm	AC coupled 50Ω Matched
3	VD	111x111µm	Drain Power Supply voltage, bypass capacitors needed*
4	VG	111x111µm	No connect, Optional Gate Power Supply voltage
5	VG2	111x111µm	No connect, Optional Gate Power Supply voltage
Die Bottom	GND	Backside	Epoxy/Solder to Baseplate

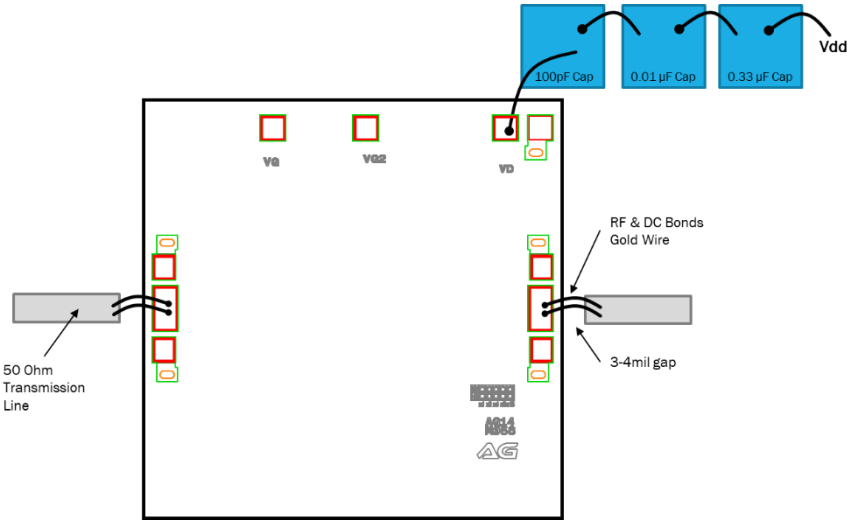
*See Assembly Diagram

Absolute Maximum Ratings

Parameter	Rating
Drain Bias Voltage (VDD)	+8V DC
RF Input Power (RFIN)	+20dBm*
Channel Temperature	200°C
Storage Temperature	-65 to 150°C
Operating Temperature	-55 to 85°C

*To be tested

Die Assembly Diagram

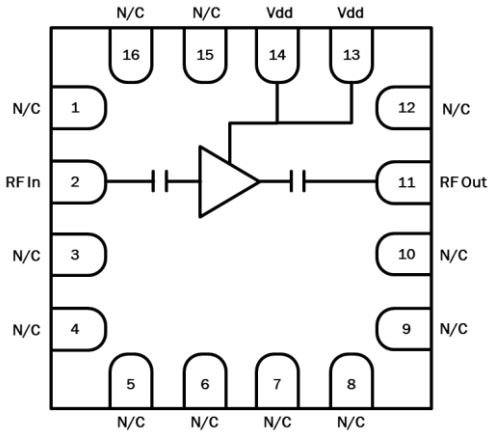


Die Assembly Notes:

1. Die Thickness is 100µm
2. Backside and Bondpad metallization: 3µm gold
3. Silver Epoxy or AuSn Eutectic attach MMIC
4. Gap between MMIC and 50 Ohm lines should be 3-4mils
5. Off-Chip bypass capacitor values are approximate



QFN Packaging Information

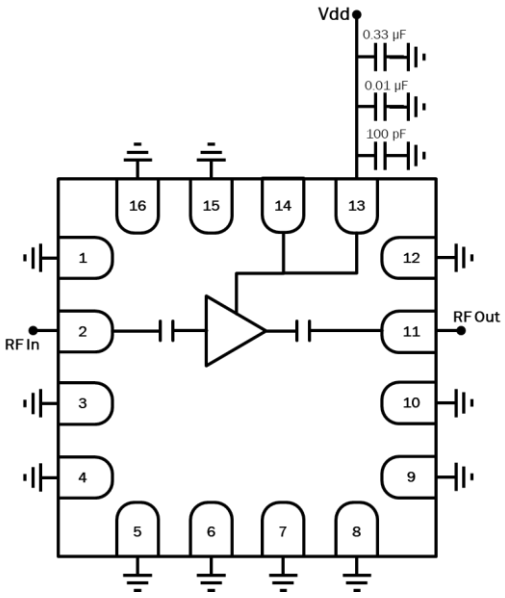


QFN Pin Descriptions

Pin	Function	Description
2	RFIN	AC coupled 50Ω Matched
11	RFOUT	AC coupled 50Ω Matched
13, 14	Vdd	Drain Power Supply voltage, bypass capacitors needed*
1,3-10,12,15,16	N/C	No connect, recommend connect to RF/DC GND
QFN Paddle	GND	Epoxy/Solder to RF/DC GND

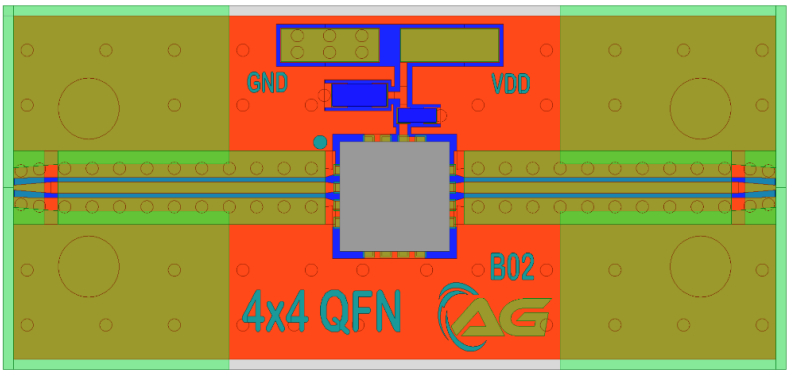
*See Application Circuit

Application Circuit



Evaluation Board*

*Gerber files available upon request



Layer	Dimension
Cu Top	½ oz
Rogers 4003	8.7mil
Cu Bottom	½ oz

Important Notice

The information contained in this Data Sheet and any associated documents is believed to be reliable; however, AmpliTech makes no warranties regarding the Data Sheet Information and assumes no responsibility of liability whatsoever for the use of the said information. All Data Sheet information is subject to change without notice.